Latch-Up Detection And Cancellation In CMOS VLSI Circuits By Phillippe O. Pouliquen

By Phillippe O. Pouliquen

Analog Devices New Product Express | DigiKey -
AD9361: RF Agile Transceiver. Blind spot detection; Self-parking; Electronic bumper; AD8284 . High Voltage Latch-Up Proof, Single SPDT Switch.
http://www.digikey.com/product-highlights/us/en/analog-devices-npe-vol6/4032

Latch- up free 600V SOI Gate Driver IC for Medium -
Latch-up free 600V SOI Gate Driver IC for Medium Power and High Temperature charge pumps for power supply and V CE detection diodes. Click here to cancel reply.
https://www.powerguru.org/latch-up-free-600v-soi-gate-driver-ic-for-medium-power-and-high-temperature-applications/

Patent US5424881 - Synchronous read channel - -
together with the error-tolerant sync mark detection and the ability to Latch-up recovery in - Terms of Service - About Google Patents
http://www.google.com/patents/US5424881

SQL Server Latch & Debugging latch time out -
Used during read IO during write IO when torn page detection Time out occurred while waiting for buffer latch Break up of above warning. type . The latch
http://mssqlwiki.com/2012/09/07/latch-timeout-and-sql-server-latch/

Yikun Chang | LinkedIn -
View Yikun Chang's professional profile on LinkedIn. Comparator and offset cancellation structure & phase; MDAC; offset and latch-up.
https://www.linkedin.com/pub/yikun-chang/86/920/764

A low leakage power-rail ESD detection circuit -
A low leakage power-rail ESD detection circuit with a modified RC network for a 90-nm A novel latch-up free SCR-LDMOS with high holding voltage for a power-rail
http://iopscience.iop.org/1674-4926/34/4/045010?recenthistorytab=viewed

IGBT Gate Driver Solutions for Low and Medium -
as well as the integration of additional blocks such as bootstrapdiodes or charge pumps for power supply and V CE detection Latch Up Immunity cancel reply
http://www.powerguru.org/igbt-gate-driver-solutions-for-low-and-medium-power-applications/

Hi-Reliability Microelectronics , Inc.: Private -
Hi-Reliability Microelectronics , Inc. company research & investing information. ESD, and latch-up services. Cancel. Submit. Your requested
http://www.bloomberg.com/research/stocks/private/snapshot.asp?privcapid=42625671

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Phillippe O. Pouliquen - Latch-Up Detection and Cancellation in CMOS VLSI Circuits jetzt kaufen. Kundrezensionen und 0.0 Sterne.
http://www.amazon.de/Latch-Up-Detection-Cancellation-CMOS-Circuits/dp/B00JBMFXFU

Jorge L Salcedo, Inventor, Allen, TX - PatentBuddy -
Jorge L Salcedo's Inventor profile, Allen, TX, TEXAS INSTRUMENTS INCORPORATED;, 2 patents/applications from Dec 29, 2003 to Dec 29, 2003, 7 forward patent citations
http://www.patentbuddy.com/Inventor/Salcedo-Jorge-L/956600

7th European Conference on POWER by liuqingzhan -
7th European Conference on POWER.doc Download legal documents
http://www.docstoc.com/docs/34130849/7th-European-Conference-on-POWER

Hirel micro - Parts Management Santa Clara CA, -
HRM has expanded its services to include comprehensive parts management, counterfeit detection and material verification, ESD and Latch-up etc.
http://www.manta.com/c/mttcxl1/hirel-micro-parts-management

Amazon.fr: Phillippe O. Pouliquen: Livres, -
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http://www.amazon.fr/Phillippe-O.-Pouliquen/e/B00LLKSKOG

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http://www.amazon.com/Phillippe-O.-Pouliquen/e/B00LLKSKOG/

IEEE Xplore - Conference Table of Contents -
Frequency degradation is monitored with a beat frequency detection system of 52dBc up to Nyquist up to 23Gb/s through ISI cancellation in the input latch
http://ieeexplore.ieee.org/xpl/tocresult.jsp?sortType%3Dasc_p_Sequence%26filter%3DAND(p_IS_Number%3A5205281)%26pageNumber%3D2%26rowsPerPage%3D75&pageNumber=1

Catastrophic Failure and Fault Tolerant Design of -
Catastrophic Failure and Fault Tolerant Design of IGBT Power Electronic Converters an Overview - Free download as PDF File (.pdf), Text file (.txt)
https://www.scribd.com/doc/259206781/Catastrophic-Failure-and-Fault-Tolerant-Design-of-IGBT-Power-Electronic-Converters-an-Overview

Patent US4625331 - Automatic frequency control -
decoder incorporates a comparator which is referenced to the mean value of the data signal so as to avoid comparator "latch-up cancellation; thus, detection
http://www.google.co.in/patents/US4625331

Lesson(s) Learned: Fault Protection - NASA -
Management and coordination of fault detection, "Safing" is defined as a general purpose fault response which results in the cancellation of non (latch-up
http://llis.nasa.gov/lesson/772

Voltage Regulator Circuit For Suppressing Latch- -
Voltage Regulator Circuit For Suppressing Latch-up Cancel. Embed document. Back to invention comprises voltage detection means which, following a "latch up
http://www.docstoc.com/docs/48904796/Voltage-Regulator-Circuit-For-Suppressing-Latch-up-Phenomenon---Patent-6184664

Publications 2002-1997 -
Publications 2002-1997. Publications 1996-1991
https://www.ims-bordeaux.fr/fr/recherche/publications-2002-1997

Chapter 5 GPS Based Relative Navigation -
navigation bene ts from a high level of common error cancellation. may further be protected by an error detection and a latch-up protection must be
http://link.springer.com/content/pdf/10.1007/978-1-4614-4541-8_5.pdf

Latch-Up Detection and Cancellation in CMOS VLSI -
ADA399884. Title : Latch-Up Detection and Cancellation in CMOS VLSI Circuits. Descriptive Note : Final technical rept. 1 Jun 1999-20 Jun 2000. Corporate Author
http://oai.dtic.mil/oai/oai?verb=getRecord&metadataPrefix=html&identifier=ADA399884

Delbert R Cecchi, Inventor, Rochester, MN, US - -
Delbert R Cecchi's Inventor Triple-well CMOS devices with increased latch-up immunity and methods 2008: Method and apparatus for detection and prevention of
http://www.patentbuddy.com/Inventor/Cecchi-Delbert-R/165545

sceas.csd.auth.gr -
sceas.csd.auth.gr
http://sceas.csd.auth.gr/php/conferences.php4?conf_id=13454

Philippe O. Pouliquen - Padgett-martin Technology -
Award Title Agency Phase Award amount Start Date End Date; Latch-Up Detection and Cancellation in CMOS VLSI Circuits Padgett-martin Technology Principal Investigator
https://sbirsource.com/sbir/people/18856-philippe-o-pouliquen